ABSTRACT OF THE DISCLOSURE

A switching I/O node for connection in a multiprocessor computer system. An input/output node switch includes a bridge unit and a packet bus switch unit implemented on an integrated circuit chip. The bridge unit may receive a plurality of peripheral transactions from a peripheral bus and may transmit a plurality of upstream packet transactions corresponding to the plurality of peripheral transactions. The packet bus switch may receive the upstream packet transactions on an internal point-to-point packet bus link and may determine a destination of each of the upstream packet transactions. The packet bus switch may further route selected ones of the upstream packet transactions to a first processor interface coupled to a first point-to-point packet bus link and route others of the upstream packet transactions to a second processor interface coupled to a second point-to-point packet bus link in response to determining the destination each of the upstream packet transactions.